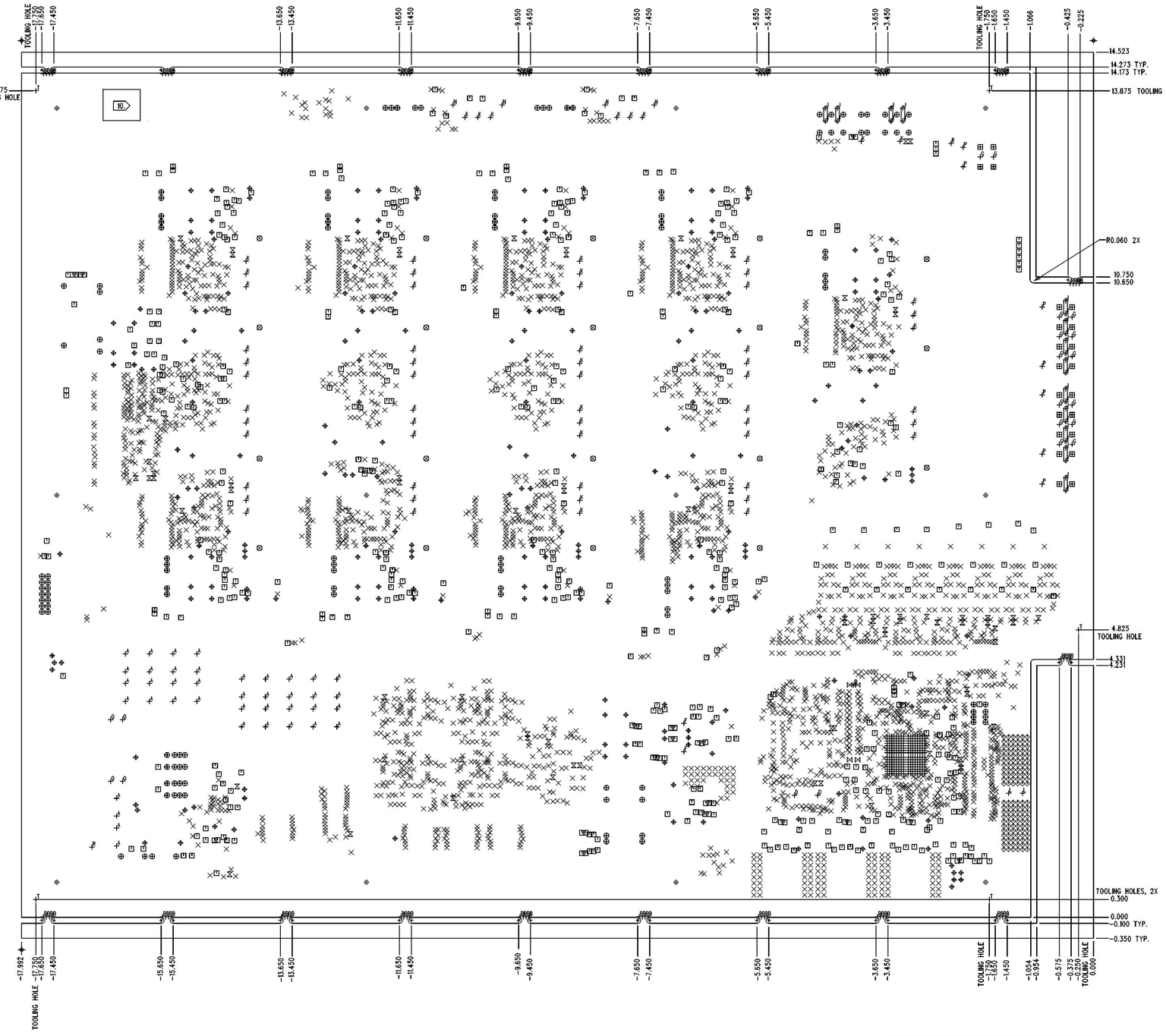
REV	REVISION DESCRIPTION	ECO NO	DATE	SIGNATURE

PCB FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

1. PRIMARY SIDE SHOWN.
2. TEN LAYER PCB.
3. FABRICATE PER IPC-6012, CLASS 2, CURRENT REV.
4. DETERMINE ACCEPTABILITY PER IPC-A-600, CURRENT REV.
   25% BREAKOUT PERMITTED ON VIAS IF INTERFACE
   BETWEEN CONDUCTOR AND TERMINAL AREA OF PAD IS 100%.
   BOARDS TO BE 100% ELECTRICALLY TESTED FOR CONTINUITY
   (OPENS AND SHORTS).
   CERTIFICATION OF THIS TEST REQUIRED
   WITH EACH SHIPMENT FOR EACH DATE CODE SUPPLIED. CERTIFICATION TO
   INCLUDE P.O. #, P/N, AND QUANTITY OF EACH DATE CODE.
5. PCBs SHALL BE RoHS COMPLIANT. MATERIAL TO BE 170 Tg FR4 OR FR406.
   BOARD TO BE 0.093" +/- 10%, MEASURED OUTER METAL-TO-METAL THICKNESS.
   BOARD FINISH TO BE LEAD FREE HASL OR ENIG. PCB SHALL BE MARKED PER
   J-STD-609 PARA 7.2 (FINAL FINISH DESIGNATOR), OR PER IPC-1066.
6. PLATE TO 1.0 OZ COPPER NOMINAL ON SURFACE LAYERS, 1.0 OZ
   COPPER NOMINAL IN HOLES AND INTERNAL PLANE LAYERS, 0.5 OZ INTERNAL
   TRACE LAYERS.
7. TOOLING HOLES OF DIAMETER UP TO 0.126" ARE NON-PLATED AND MAY
   OR MAY NOT BE PRESENT IN DESIGN AS PER SUPPLIED ARTWORK.
   IF PRESENT IN DESIGN THEY SHALL BE MARKED "T". ALL OTHER HOLES
   SHALL BE PLATED OR NON-PLATED ACCORDING TO HOLE CHART.
8. HOLE SIZES GIVEN ARE FINISHED DIMENSIONS.
9. SOLDERMASK BOTH SIDES OVER BARE COPPER PER IPC-SM-840,
   CLASS 2, CURRENT REV, AND MANUFACTURERS SPECIFICATIONS.
   NO BARE COPPER ALLOWED. NO SOLDER MASK
   PERMISSIBLE ON COMPONENT PADS AS PER SUPPLIED ARTWORK.
10. DATE CODE, UL RECOGNIZED VENDOR MARK, AND UL94V-0 MARK REQUIRED.
    DATE CODE SHALL USE FOUR NUMERALS, GIVING WORK WEEK
    AND YEAR, EG., 2818 STANDS FOR THE 28TH WEEK OF 2018.
    THESE MARKS SHALL BE MADE IN COPPER AND SHALL BE LOCATED
    ON THE SECONDARY SIDE OF THE PCB.
11. SCREEN COMPONENT ID WITH NON-CONDUCTING WHITE INK.
    COMPONENT ID REGISTRATION TO BE WITHIN +/- 0.005" OF ITS
    RESPECTIVE COMPONENT LAYER.
    NO SILKSCREEN INK PERMISSIBLE ON COMPONENT PADS
    OR IN PADS AS PER SUPPLIED ARTWORK.
12. ETCH TOLERANCE +0.001" - 0.002". TOTAL TRACE REDUCTION
    CANNOT EXCEED 20%.
13. FRONT-TO-BACK REGISTRATION TO BE WITHIN +/-0.003".
14. BOARD WARP TO BE NO GREATER THAN 1.2%.
15. CONTROLLED IMPEDANCE AT 10% TOLERANCE. TRACE WIDTH MAY
    BE ADJUSTED TO MEET IMPEDANCE REQUIREMENTS, BUT NOT BELOW
    0.0045" IN WIDTH OR CLEARANCE:
    0.005" TRACES ON ALL LAYERS ARE 100 OHM DIFFERENTIAL
16. LAYER CONFIGURATION DIAGRAM:
    PRIMARY SIDE COMPONENT I.D.
    PRIMARY SIDE SOLDER MASK
    CIRCUIT LAYER #1 (PRIMARY SIDE)
    CIRCUIT LAYER #2 – PLANE LAYER
    CIRCUIT LAYER #3 – TRACE LAYER
    CIRCUIT LAYER #4 – PLANE LAYER
    CIRCUIT LAYER #5 – PLANE LAYER
    CIRCUIT LAYER #6 – PLANE LAYER
    CIRCUIT LAYER #7 – PLANE LAYER
    CIRCUIT LAYER #8 – TRACE LAYER
    CIRCUIT LAYER #9 – PLANE LAYER
    CIRCUIT LAYER #10 (SECONDARY SIDE)
    SECONDARY SIDE SOLDER MASK
    SECONDARY SIDE COMPONENT I.D.

MINIMUM INNER LAYER SPACING IS 0.005" MEASURED BETWEEN ANY TWO COPPER LAYERS.



SIZE	QTY	SYM	PLATED	TOL
0.01	256	+	YES	+0.000/-0.010
0.012	3229	×	YES	+0.000/-0.012
0.021	499	□	YES	+0.000/-0.021
0.024	132	◇	YES	+/-0.002
0.025	82	⧖	YES	+/-0.003
0.028	4	⋈	YES	+/-0.003
0.03	40	A	YES	+/-0.003
0.033	81	B	NO	+/-0.003
0.035	127	⊕	YES	+/-0.003
0.039	2	C	NO	+/-0.003
0.04	253	⌖	YES	+/-0.003
0.05	2	D	NO	+/-0.003
0.052	4	E	YES	+/-0.005
0.06 x 0.275	13	F	NO	+/-0.003
0.065	14	G	NO	+/-0.003
0.065	22	⊞	YES	+/-0.005
0.07	62	H	YES	+/-0.005
0.079	2	I	NO	+/-0.005
0.1	4	J	YES	+/-0.003
0.118	7	K	NO	+/-0.003
0.125	2	L	NO	+/-0.007
0.125	19	⊗	YES	+/-0.007
0.126	5	M	NO	+/-0.003
0.1378	12	◈	YES	+/-0.007

SOLDER OR PLATING PLUG ACCEPTABLE IN HOLES UP TO 0.021"

PCB PRIME

PCB Prime Sample Fabrication Drawing

THIRD ANGLE PROJECTION	ADDITIONAL INFORMATION AND SPECIFICATIONS REQUIRED TO MANUFACTURE THIS PART PROVIDED			PCB Prime Sample Fabrication Drawing 13900 E Florida Ave, Suite F, Aurora CO 80012 USA
	UNLESS OTHERWISE SPECIFIED: ALL DRAFTING PRACTICES BASED ON ANSI DRAFTING STANDARDS ALL DIMENSIONS ARE IN INCHES			TITLE Really Big Board With Tab Routing
	DFTR Scott Walsh	10.15.2018	TOLERANCES UNLESS OTHERWISE NOTED	
	CHKD		.X	
	APVD		.XX +/- .005	DWG SIZE D
M/P NEXT ASSY USED.ON	APVD		ANGULAR	PART NO 123456 / SCALE / SHEET 1 OF 1 / REV A